Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 2, 10, 11, 18, 22, 24 and 28 have been amended. No claims have been cancelled. Therefore, claims 1-29 are presented for examination.

In the Office Action, the Drawings have been objected to by the Draftsperson. Applicant will provide formal drawings upon allowance of the application. In addition, Figure 1 is objected to because Figure 1 does not include a legend as suggested by the Examiner. Applicant submits that Figure 1 has been amended as suggested by the Examiner.

Figures 2, 3 and 4 have been objected under 37 CFR 1.84(p)(4) for not including reference numbers for various lines/inputs that have not been discussed in the Specification. Applicant submits that there is no requirement in 37 CFR 1.84 that all descriptors in a Figure include a reference character. Similarly, there is no need to describe descriptors in the Specification that do not include reference characters in the Figure.

In fact, 37 CFR 1.84(p)(5) requires that reference characters not mentioned in the description shall not appear in the drawings, and that reference characters mentioned in the description shall appear in the drawings. Therefore, applicant submits that in those instances in Figures 2, 3 and 4 where reference characters are not mentioned in the description, reference characters are not required in the drawings. The instances in Figures 3 and 4 where a reference character is not described in the description has been deleted from Figures 3 and 4.

Claims 1-29 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, the Examiner asserts that the term "data access primitive" used in the claims is not adequately described, nor enabled by the specification.

Applicant submits that the present application is properly enabled. Data access primitives are described with reference to Figures 2, 3 and 4. In particular, the application describes that data access primitives are logic design components that may be used by a designer to specify an assembly of address and lane matching logic. Such logic is described in Figure 1. In addition, the data access primitives hide the details of interconnection to a bus, and abstracts away the interdependency of address-matching functions, lane-matching functions and data bus connections. See Specification at page 7, lines 4-10.

Moreover, the Specification discloses that data access primitives are converted by a data access technology mapper to low level logic components in order to implement the address-matching functions, lane-matching functions and data bus connections. Id. At page 9, line 14 – page 11, line 5. Therefore, the present claims are properly enabled.

Claims 1-29 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claims the subject matter which application regards as invention. Particularly, the Examiner asserts that the term "data access primitive" used in the claims is not adequately defined in the specification.

Examiner submits that "data access primitive" is adequately defined in the Specification. It has long been established that an applicant may be his or her own lexicographer, so long as a term in a claim is not given a meaning repugnant to the usual meaning of that term. In re Hill, 161 F.2d 367, 73 USPQ 482. As discussed above, data access primitives are described as logic design components that may be used by a designer to specify an assembly of address and lane matching logic. Further, each data access primitive implies address-matching functions, lane-matching functions, and data bus connections for one or more bytes of data and auxiliary logic. See Specification at page 7, lines 4-15. Therefore, the term "data access primitive" is properly defined in the Specification.

Claims 1-4, 6-13, 15-18, 20-24, and 26-29 stand rejected under 35 U.S.C. §102(b) as being anticipated by Advanced Microprocessors of Tabak ("Tabak"). Applicant submits that the present claims are patentable over Tabak.

Tabak discloses various microprocessor architectures. However, claim 1 of the present application recites converting a data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for a memory-mapped device based upon the data access primitive and a first starting address. Applicant submits that nowhere in Tabak is there disclosed a data access primitive as recited in claim 1. Moreover, there is no disclosure of converting such a data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for a memory-mapped device. Accordingly, claim 1 is patentable over Tabak.

Claims 2-9 depend from claim 1 and include additional limitations. Thus, claims 2-9 are also patentable over Tabak

Claim 10 recites converting a data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for a memory-mapped device based upon the data access primitive and a first starting address. Thus, for the reasons described above with respect to claim 1, claim 10 is also patentable over Tabak. Because claims 11-17 depend from claim 10 and include additional limitations, claims 11-17 are also patentable over Tabak.

Claim 18 recites generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections. There is no disclosure in Tabak of generating logic components that implement address matching and lane matching functions, or one or more bus connections. Therefore, claim 18 is also patentable over Tabak. Since claims 19-23 depend from claim 18 and include additional limitations, claims 19-23 are also patentable over Tabak.

Claim 24 recites generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections. Thus, for the reasons described above with

respect to claim 18, claim 24 is also patentable over Tabak. Since claims 25-29 depend from claim 24 and include additional limitations, claims 25-29 are also patentable over Tabak.

Claims 5, 14, 19, and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tabak in view of applicant's admission. Applicant submits that the present claims are patentable over Tabak even in view of background pf the application.

Applicant's background discloses specifying the addressability and bus connections, and the tediousness of a designer to explicitly specify designing for 8-bit and 32-bit system busses. See Specification at pages 1 and 2. However, if anything, applicant's background teaches away from the claims since the claims recite generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections.

As described above, Tabak does not disclose or suggest such a limitation. Therefore, the present claims are patentable over any combination of Tabak and applicant's background since neither disclose nor suggest generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections.

Applicant respectfully submits that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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Version with Markings to Show Changes Made

Insertions are underlined, deletions are stricken.

1. (Amended) A method[of addressing a memory-mapped device,] comprising:

using a data access primitive to model addressability for [the] a memory-mapped device, addressability comprising an address matching function, a lane matching function and one or more bus connections,

specifying a first starting address for the memory-mapped device; and

[generating] converting the data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device [using] based upon the data access primitive and the first starting address.

2. (Amended) The method of claim 1, further comprising [generating] converting the data access primitive to logic components that implement a second set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device [using] based upon the data access primitive and a second starting address.

10. (Amended) A computer readable medium containing executable instructions which, when executed in a processing system, causes the processing system to perform[the steps of] a method comprising:

using a data access primitive to model addressability for [the] a memory-mapped device, addressability comprising an address matching function, a lane matching function and one or more bus connections,

specifying a first starting address for the memory-mapped device; and

[generating] converting the data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device [using] based upon the data access primitive and the first starting address.

11. (Amended) The computer readable medium of claim 10, further comprising [generating] converting the data access primitive to logic components that implement a second set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device [using] based upon the data access primitive and a second starting address.

18. (Amended) A method, comprising:

selecting a data access primitive [that] to provide data access of a desired transaction size, [the data access primitive implying] and to indicate an addressing matching function, a lane matching function and one or more bus connections for a memory-mapped device;

specifying an address constraint for the memory-mapped device;

instantiating a logic for the memory-mapped device, comprising:

generating a starting address for the memory mapped device using the address constraint;

using the selected data access primitive and the starting address to map the logic for the memory mapped device capable of being accessed at the desired transaction size, comprising:

generating first logic components that implement the address matching function, and

generating second logic components that implement the lane matching function and the one or more bus connections.

22. (Amended) The method of claim 21, wherein [a] different logic for the memory mapped device is instantiated automatically using the same data access primitive and the new starting address.

24. (Amended) A computer readable medium containing executable instructions which, when executed in a processing system, causes the processing system to perform[the steps of] a method, comprising:

selecting a data access primitive [that] to provide data access of a desired transaction size, [the data access primitive implying] and to indicate an addressing matching function, a lane matching function and one or more bus connections for a memory-mapped device;

specifying an address constraint for the memory-mapped device;

instantiating a logic for the memory-mapped device, comprising:

generating a starting address for the memory mapped device using the address constraint;

using the selected data access primitive and the starting address to map the logic for the memory mapped device capable of being accessed at the desired transaction size, comprising:

generating first logic components that implement the address matching function, and

generating second logic components that implement the lane matching function and the one or more bus connections.

28. (Amended) The computer readable medium of claim 27, wherein [a] different logic for the memory mapped device is instantiated automatically using the same data access primitive and the new starting address.